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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,181	01/28/2004	David James Seal	550-505	9851

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EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,181	SEAL ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-13,15-22 and 24-27* is/are rejected.

7)☒ Claim(s) *5,14 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/28/2004*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

10/26/05.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statements (IDSs) submitted on January 28, 2004 and October 26, 2005 have considered by the examiner.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 19-27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. As the claims directed to computer program product, which can be descriptive material, and not embodied as a computer readable storage medium, it can be considered as descriptive material and therefore unpatentable.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 6-13, 15-22, and 24-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Mahon et al. (Hewlett-Packard Precision Architecture: The Processor. Published: August 1988) (Mahon herein after).

As per claim 1, Mahon teaches apparatus for processing data (page 5, fig. 1), said apparatus comprising:

a register bank having one or more registers operable to hold respective data values (page 5, fig. 2);

a data access circuit operable to perform data access operations transferring one or more data values between said apparatus and addressed memory locations within a memory circuit (page 5, fig.1, column 1, paragraph 2); and

an instruction decoder responsive to data access program instructions to control said data circuit to perform respective data access operations, each of said data access program instructions including an address offset field that specifies an offset value and including a base register field that specifies a base register within said register bank and specifying a manipulation to be performed upon said offset value and a base address value held in said base address register to form a memory address value to be accessed within said memory circuit upon execution of said data access program instruction (page 5, column 1, paragraphs 2-3, taught as execution unit performs data transformations and moves data between memory system and fetch unit fetches the instruction and decodes it. Also on page 7, column 1, paragraph 2 and column 2,

paragraph 5, teaches that all address calculation in LOAD and STORE instructions is based on the base register plus displacement addressing mode); wherein

said data access program instructions have:

(i) a first form including an address offset field having a first address offset filed length (page 20, fig. 8, first instruction labeled as LD/ST L); and

(ii) a second form including an address offset field having a second address offset field length (page 20, fig. 8, second instruction labeled as LD/ST S/X), said first address field length being greater than said second address offset field (page 7, column 2, paragraph 5, taught as displacement can be long 14-bit or a short 5-bit) and said first form being capable of specifying a lesser number of possible manipulations to be performed upon said base address value and said offset value than said second form (page 7, column 2, paragraph 5, page 19, column 1, paragraph 8 to column 2, paragraphs 1-2 and page 20, fig. 8, shows two types of LOAD/STORE instructions and depending on their respective bit values first instruction can perform base value plus displacement value and second instruction with sub-opcode and short displacement can perform base address value plus displacement, or index register).

As per claim 2, Mahon teaches adding and subtracting offset values from base address value (page 7, column 2, paragraph 5).

As per claim 3, Mahon teaches manipulation also allows at least one of the following options for a data access operation:

using said base address value as said memory address value;

using said modified address value as said memory address value;

using said base address value and writing back said unmodified address value to said base address register as said memory address value; and

using said modified address value and writing back said modified address value to said base address register as said memory address value (page 7, column 2, paragraphs 5-6, Mahon teaches base address plus signed displacement and use of index register and use of base register for a subsequent load or store operation and pre-modification and post-modification).

As per claim 4, Mahon teaches access control as privilege level (page 15, column 2, paragraph 4).

As per claim 6, Mahon teaches modification specifier (page 20, fig. 8, page 7, column 2, paragraph 7).

As per claim 7, Mahon teaches second form including manipulation mode control field specifying which of plurality of different manipulations (page 19, column 1, paragraph 8, taught as subop field).

As per claim 8, Mahon teaches instructions are disjoint (page 7, column 2, paragraph and page 9, column 1, paragraph 1).

As per claim 9, Mahon teaches data values are transferred between registers and memory (page 5, figs. 1 and 2 and column 1, paragraphs 2-3 and column 2, paragraphs 2-3).

Claims 10-13, 15-22 and 24-27 are rejected under same rationales as applied to claims 1-4 and 6-9 above.

Allowable Subject Matter

7. Claims 5, 14 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

Mano Padmanabhan 5/24/06
MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER